What is claimed is:

1. A synchronous type semiconductor memory device comprising:

a memory cell array in which memory cells are arranged in a matrix;

a row address decoder which activates one of word lines in said memory cell array based on a row address in response to a word activation signal;

a column decoder which activates one of bit line pairs in said memory cell array based on a column address ;

a sense amplifier circuit which amplifies a voltage difference on said activated bit line pair in response to a sense amplifier activation signal;

a clock data storage section which stores clock data showing a frequency or period of an external clock signal; and

a control section which generates said word activation signal based on a row address strobe signal, and generates said sense amplifier activation signal based on said clock data and said row address strobe signal in response to an internal clock signal synchronous with said external clock signal.

2. The synchronous type semiconductor memory device according to claim 1, wherein said control section comprises:

an operation timing signal generating section which receives said row address strobe signal, generates said word activation signal based on said row address strobe signal, and generates a plurality of candidate sense amplifier activation signals based on said row address strobe signal in response to said internal clock signal; and

a selecting section which selects one of said plurality of candidate sense amplifier activation signals as said sense amplifier activation signal based on said clock data.

3. The synchronous type semiconductor memory device according to claim 2, wherein said operation timing signal generating section comprises:

a buffer which receives said row address strobe signal, and outputs said word activation signal; and

a sequence of delay elements which shifts said row address strobe signal in response to said internal clock signal, and outputs said plurality of candidate sense amplifier activation signals from different ones of said delay elements.

4. The synchronous type semiconductor memory device according to claim 3, wherein each of said delay elements is a flip-flop.

5. The synchronous type semiconductor memory device according to claim 4, wherein at least one of said delay elements is triggered by a falling edge of said internal clock signal and remaining ones of said delay elements are triggered by a rising edge of said internal clock signal.

6. The synchronous type semiconductor memory device according to claim 1, further comprising:

a data amplifier which amplifies and outputs data corresponding to the amplified voltage difference on said activated bit line pair in response to a data amplifier activation signal,

wherein said control section generates said data amplifier activation signal based on said clock data and a column address strobe signal in response to said internal clock signal.

7. The synchronous type semiconductor memory device according to claim 6, wherein said control section comprises:

an operation timing signal generating section which receives said row address strobe signal, generates said word activation signal based on said row address strobe signal, generates a plurality of candidate sense amplifier activation signals based on said row address strobe signal in response to said

internal clock signal, and generates a plurality of candidate data amplifier activation signals based on said column address strobe signal in response to said internal clock signal; and

a selecting section which selects one of said plurality of candidate sense amplifier activation signals as said sense amplifier activation signal based on said clock data, and selects one of said plurality of candidate data amplifier activation signals as said data amplifier activation signal based on said clock data.

8. The synchronous type semiconductor memory device according to claim 7, wherein said operation timing signal generating section comprises:

a buffer which receives said row address strobe signal, and outputs said word activation signal;

a sequence of first delay elements which shifts said row address strobe signal in response to said internal clock signal, and outputs said plurality of candidate sense amplifier activation signals from different ones of said first delay elements; and

a sequence of second delay elements which shifts said column address strobe signal in response to said internal clock signal, and outputs said plurality of candidate data amplifier activation signals from different ones of said second delay

elements.

9. The synchronous type semiconductor memory device according to claim 8, wherein each of said first and second delay elements is a flip-flop.

10. The synchronous type semiconductor memory device according to claim 9, wherein at least one of said first delay elements is triggered by a falling edge of said internal clock signal and remaining ones of said first delay elements are triggered by a rising edge of said internal clock signal, and

at least one of said second delay elements is triggered by a falling edge of said internal clock signal and remaining ones of said second delay elements are triggered by a rising edge of said internal clock signal.

11. A method of accessing a memory cell array in a synchronous type semiconductor memory device, said method comprising:

(a) generating a word activation signal based on a row address strobe signal;

(b) generating a sense amplifier activation signal based on clock data, showing a frequency or period of an external clock signal, and said row address strobe signal in response to an internal clock

signal synchronous with said external clock signal;

(c) activating one of word lines based on a row address in response to said word activation signal;

(d) activating one of bit line pairs based on a column address; and

(e) amplifying data corresponding to said activated bit line pair and said activated word line in response to said sense amplifier activation signal.

12. The method according to claim 11, wherein said (b) generating comprises:

(f) generating a plurality of candidate sense amplifier activation signals based on said row address strobe signal in response to said internal clock signal; and

selecting one of said plurality of candidate sense amplifier activation signals as said sense amplifier activation signal based on said clock data.

13. The method according to claim 12, wherein said (f) generating comprises:

shifting said row address strobe signal in a sequence of first delay elements in response to said internal clock signal; and

outputting said plurality of candidate sense amplifier activation signals from different ones of said first delay elements.

14. The method according to claim 13, wherein each of said first delay elements is a flip-flop.

15. The method according to claim 14, wherein at least one of said first delay elements is triggered by a falling edge of said internal clock signal and remaining ones of said first delay elements are triggered by a rising edge of said internal clock signal.

16. The method according to claim 11, further comprising:

(g) generating a data amplifier activation signal based on said clock data and a column address strobe signal in response to said internal clock signal; and

amplifying said amplified data in response to said data amplifier activation signal.

17. The method according to claim 16, wherein said (g) generating comprises:

(h) generating a plurality of candidate data amplifier activation signals based on said column address strobe signal in response to said internal clock signal; and

selecting one of said plurality of candidate data amplifier activation signals as said data

amplifier activation signal based on said clock data.

18. The method according to claim 17, wherein said (h) generating comprises:

shifting said column address strobe signal in a sequence of second delay elements in response to said internal clock signal; and

outputting said plurality of candidate data amplifier activation signals from different ones of said second delay elements.

19. The method according to claim 18, wherein each of said second delay elements is a flip-flop.

20. The method according to claim 19, wherein at least one of said second delay elements is triggered by a falling edge of said internal clock signal and remaining ones of said second delay elements are triggered by a rising edge of said internal clock signal.